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Title:

AN OPTIMIZED PHOTODIODE PROCESS FOR IMPROVED TRANSFER GATE LEAKAGE

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AN OPTIMIZED PHOTODIODE PROCESS FOR IMPROVED TRANSFER GATE LEAKAGE

FIELD OF THE INVENTION

[0001] The present invention relates to improved photodiodes used in pixels of an image array.

BACKGROUND OF THE INVENTION

[0002] CMOS image devices having pixel sensor arrays are well known in the art and have been widely used due to their low voltage operation and low power consumption. CMOS image devices further have advantages of being compatible with integrated on-chip electronics, allowing random access to the image data, and having lower fabrication costs as compared to other imaging technologies. CMOS image devices are generally disclosed for example, in Nixon et al., "256 X 256 CMOS Active Pixel Sensor Camera-on-a-Chip," IEEE Journal of Solid State Circuits, vol. 31(12) pp. 2046-2050, 1996; Mendis et al., CMOS Active Pixel Image Sensors," IEEE Transactions on Electron Devices, vol. 41(3) pp. 452-453, 1994 as well as U.S. Pat. Nos. 5,708,263, 5,471,515, and 6,291,280, which are hereby incorporated by reference.

[0003] However, conventional CMOS image devices have some significant drawbacks. When photodiode implants are formed within a semiconductor substrate of a pixel cell

adjacent a transfer transistor to transfer charge from the photodiode, the resulting structure creates leakage problems beneath the transfer gate, particularly during charge integration, when the transfer transistor is off. FIG. 1 illustrates a prior art pixel cell 750 with a n-type photodiode implant 705 set in a p-type substrate 915, wherein the implant is on one side of transfer gate 701, with a floating diffusion region 702 on the opposite side of gate 701. STI region 707 is an isolation region which isolates one pixel from another. The n-type photodiode implant 705 forms a P-N diode junction above implant 705 with the p-type material which is over implant 705.

[0004] The photodiode implant 705 is typically formed using an implant angle θ (706) in order to extend the implant slightly under gate 701 to provide sufficient conductivity between the photodiode n-region 705 and the channel region beneath transfer gate 701. Once implanted, the resulting extended photodiode n-region 705 facilitates transfer of electrons to the channel beneath gate 701 and to the floating diffusion 702 when the gate 701 is on (e.g., a positive voltage applied which is greater than the threshold of the transfer transistor formed by gate 701 and implant regions 702, 705). However, as is shown in FIG. 2, when transfer gate 701 is off, residual charge from n-region 705 leaks in the direction of arrows 800 beneath transfer gate 701 to floating diffusion region 702. This is due to the fact that the shallow angled implant results in a shape for n-region 705, where a portion of the photodiode is in very close proximity to the transfer gate 701. This proximity, while providing a good charge transfer when gate 701 is on, has the unwanted by-product of some undesirable charge leakage when the gate 701 is

off. Accordingly, a better photodiode implant which provides good charge transfer when gate 701 is on, while lowering leakage when gate 701 is off is needed.

BRIEF SUMMARY OF THE INVENTION

[0005] The present invention provides a CMOS imager having a pixel array in which each pixel has an improved photodiode implant. The photodiode implant is created by tailoring the angle of a plurality of charge collection region implants so that the resulting charge collection region is positioned to provide a good charge transfer characteristic when the transfer transistor gate is on and lowered leakage across the channel region when the transistor gate is off. The photodiode charge collection region is formed through the successive implants into the substrate, some of which are angled, to minimize the barrier and in turn minimize the leakage.

[0006] The above and other advantages and features of the invention will be more clearly understood from the following detailed description which is provided in connection with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] FIG. 1 shows a partially cut away side view of a prior art angled diode implant in a semiconductor imager;

[0008] FIG. 2 illustrates the leakage occurring beneath transfer gate 701 in the FIG. 1 arrangement;

[0009] FIG. 3A shows a first reduced-angle diode implant in accordance with a first embodiment of the invention;

[0010] FIG. 3B shows a second reduced-angle diode implant in accordance with the first embodiment of the invention;

[0011] FIG. 3C shows a third reduced-angle diode implant in accordance with the first embodiment of the invention;

[0012] FIG. 3D shows a supplemental implant to the reduced-angle diode implant in accordance with a second embodiment of the invention;

[0013] FIG. 4 illustrates an electrostatic potential contour of the diode/transfer gate region formed in a substrate and the donor concentrations in accordance with a third embodiment of the invention;

[0014] FIG. 5 illustrates an electrostatic potential contour of the diode/transfer gate region formed in a substrate and the donor concentrations in accordance with a fourth embodiment of the invention;

[0015] FIG. 6 illustrates an electrostatic potential contour of the diode/transfer gate region formed in a substrate and the donor concentrations in accordance with a fifth embodiment of the invention;

[0016] FIG. 7 illustrates an electrostatic potential contour of the diode/transfer gate region formed in a substrate and the donor concentrations in accordance with a sixth embodiment of the invention;

[0017] FIG. 8 illustrates an electrostatic potential contour of the diode/transfer gate region formed in a substrate and the donor concentrations in accordance with a seventh embodiment of the invention; and

[0018] FIG. 9 is an illustration of a computer system having a CMOS imager according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0019] In the following detailed description, reference is made to the accompanying drawings which form a part hereof, and in which is shown by way of illustration specific embodiments in which the invention may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized, and that structural, logical and electrical changes may be made without departing from the spirit and scope of the present invention.

[0020] The terms "wafer" and "substrate" are to be understood as including silicon, silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) technology, doped and undoped semiconductors, epitaxial layers of silicon supported by a base semiconductor foundation, and other semiconductor structures. In addition, the semiconductor need not be silicon-

based, but could be based on silicon-germanium, germanium, or gallium arsenide. Furthermore, when reference is made to a "wafer" or "substrate" in the following description, previous process steps may have been utilized to form regions or junctions in the base semiconductor structure or foundation.

[0021] The term "pixel" refers to a picture element unit cell containing a photosensor and transistors for converting electromagnetic radiation to an electrical signal. For purposes of illustration, a representative pixel is illustrated in the figures and description herein, and typically fabrication of all pixels in an imager will proceed simultaneously in a similar fashion. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined by the appended claims.

[0022] Fabrication of a photodiode adjacent a transfer gate in accordance with a first embodiment of the invention will now be described. Referring to FIG. 3A, a portion of a substrate having a p-type doping region 915 is illustrated, where a photodiode will be produced. It is understood that the CMOS imager of the present invention can also be fabricated using n-doped regions in an p-well. A transfer gate stack 940 is fabricated over the substrate region 915. Any LDD source/drain implant associated with region 702 and with other transistors being fabricated on the same structure are performed and a photolithography resist 950 is then applied, having an opening 949 through which a doping implant for a photodiode can pass. The gate stack 940 contains a gate oxide and a conductor, where an insulator is placed over the conductor. The conductor may be formed

from material such as poly-silicon, silicide, metal, or a combination. The insulator may be formed from material such as oxide, nitride, metal oxide, or a combination.

[0023] FIG. 3A illustrates a first n-type diode implant (PD1) 900, formed in p-type substrate 915 through resist opening 949 at a depth indicated as 903, wherein the depth 903 is in the range of 0.1 to 0.7 microns, preferably 0.1-0.5. The dopants for the implant 900 are implanted at an angle θ_1, shown as arrow 910, towards the transfer gate 940. Angle θ_1 is measured away from a line normal to the surface of the sensor, as shown in FIG. 3A. Angle θ_1 for implant 900 is set in the range of 0-30° normal to the surface of sensor 920, preferably at 0-15°. Implant 900 is preferably a low energy implant, where the implant energy used for implant 900 is in the range of 5-200KeV, preferably less than 100KeV. The implant dose for implant 900 is in the range of 2E11 – 1E13/cm^2, preferably 1E12-6E12/cm^2.

[0024] FIG. 3B illustrates a second n-type diode implant (PD2) 901, placed in p-type substrate 915 at a depth illustrated as 904, wherein implant 901 may be set forward from implant 900 in the direction of transfer gate 940, by a distance 906 as shown in FIG. 3B. The dopants for the implant 901 are set at an angle θ_2 towards the transfer gate. Angle θ_2 is measured away from a line normal to the surface of the sensor, as shown in FIG. 3B. Angle θ_2 for implant 901 is preferably set in the range of 0-30° normal to the surface of sensor 920, preferably at 0-15°. Implant 901 is preferably a higher energy implant than that used for implant 900, where the implant energy for implant 901 is in the range of 30-

300KeV, preferably 50-250KeV. The implant dose for implant 901 is in the range of 2E11 – 1E13/cm^2, preferably 1E12-6E12/cm^2.

[0025] FIG. 3C illustrates a third n-type diode implant (PD3) 902, placed in p-type substrate 915 at a minimum depth indicated as 905, wherein implant 902 may be offset from implant 901 by a distance 907 as shown in FIG. 3B. The dopants for the diode are implanted 912 at an angle θ_3 towards the transfer gate. Angle θ_3 is measured away from a line normal to the surface of the sensor, as shown in FIG. 3B. Angle θ_3 for implant 902 is preferably set in the range of 0-30° normal to the surface of sensor 920. Implant 902 is preferably a high energy deep implant, where the implant energy for implant 902 is in the range of 60-500KeV, preferably 100-400KeV. The implant dose for implant 902 is in the range of 2E11 – 1E13/cm^2, preferably 1E12-6E12/cm^2. Once formed, the implants (900, 901, 902) of FIG. 3A-C collectively form an n-type electron collection 930 forming part of a photodiode with a p-type region 947, residing over region 930. Under the illustrations of FIGs. 3A-C, at least one of the implants must be angled.

[0026] FIG 3D illustrates an alternate embodiment of the present invention, wherein three implants 900, 901 and 902 are implanted into a p-type substrate 915. The implants 900, 901 and 902, are placed in substrate 915 in a manner similar to that described in the embodiment of FIG. 3A-C, except that the implant angle for each of the implants (θ_1, θ_2, and θ_3) is reduced to a range of 0-5°, where at least one of the implants 901 and 902 has an implant angle greater than 0°. Once the implants have been set, a fourth light implant

(PD 4) 920 is made in the region of the second 901 implant, on the side closest to the transfer gate. The fourth implant is inserted 913 at an increased angle θ_4, wherein the implant angle θ_4 is measured away from a line normal to the surface of the substrate, as shown in FIG. 3D, and is preferably in the range of 10-30° of normal. Exemplary implant doses for the fourth implant may be in the range of $2e11/cm^2$-$5e12/cm^2$. It is understood that the order of the implants (900, 901, 902 and 904 (if provided)) is not critical; each of the disclosed implants may be arranged in any order.

[0027] FIGs. 4-8 show doping profiles in a partially cut away side view of angled diode implants for the implanted photodiode region 930, wherein the various drawings illustrate the dopant concentrations resulting from different exemplary angled implants that may be used. FIG. 4 shows a diode region 930A that is formed in a substrate 915 as a result of the implant methods discussed above in FIG. 3A-C. Specifically, FIG. 4 illustrates a transfer gate 940, surrounded by an insulating layer 102, formed over a substrate 915, which also has an implant n-type floating diffusion region 702. Region 930A represents n-type charge collection region of the photodiode formed in accordance with the three-implant process described above in connection with FIGs. 3A-3C, wherein the implant angles of PD1-PD3 are set at θ_1=5° for PD1region 900 (see FIG. 3A), θ_2=5° for PD2 region 901 (see FIG. 3B), and θ_3=30° for PD3 region 902 (see FIG. 3C). FIG. 4 also shows four concentration regions (I-IV) that are formed in the substrate as a result of the three implants at the specified implant angles (θ_1=5°, θ_2=5°, and θ_3=30°).

[0028] Region I, generally defined by the region above 130 and below regions 104 and floating diffusion 702, has the largest donor concentration between the range of just over 5E16 /cm^3 to 5E17/cm^3. Region II, generally defined by the region between 125 and 130, has a lesser donor concentration between the ranges of just over 5E15/cm^3 to 5E16/cm^3. Region III, generally defined by the region between 120 and 125, has yet a smaller donor concentration between the ranges of just over 1E14/cm^3 to 5E15/cm^3. Region IV, generally defined by the region below 120, contains the lowest donor concentration at or below 1E14/cm^3. As can be seen from FIG. 4, the reduced donor concentrations found in region II near the transfer gate 940 creates a potential barrier wherein the amount of donor impurities under the transfer gate 940 is reduced. This reduction lessens the occurrence of short-channel effects or punch-through beneath the gate 940.

[0029] FIG. 5 illustrates region 930B in accordance with another embodiment of the invention. Region 930B in FIG. 5 represents the diode formed subsequent to the three-implant process described above, wherein the implant angles of PD1-PD3 are set at θ_1=5° for PD1(see FIG. 3A), θ_2=5° for PD2 (see FIG. 3B), and θ_3=15° for PD3 (see FIG. 3C). FIG. 5 also shows four concentration regions (I-IV) that are formed in the substrate as a result of the diode region 930B formed by the three implants at the specified implant angles (θ_1=5°, θ_2=5°, and θ_3=15°).

[0030] Region I, generally defined by the region above 131 and below regions 104 and floating diffusion 702, has the largest donor concentration between the range of just over 5E16 /cm^3 to 5E17/cm^3. Region II, generally defined by the region between 126 and 131, has a lesser donor concentration between the ranges of just over 5E15/cm^3 to 5E16/cm^3. Region III, generally defined by the region between 121 and 126, has yet a smaller donor concentration between the ranges of just over 1E14/cm^3 to 5E15/cm^3. Region IV, generally defined by the region below 121, contains the lowest donor concentration at or below 1E14/cm^3. As can be seen in the electrostatic potential contour illustration, the reduction of the implant angle θ_3 from 30° to 15° from the previous embodiment has resulted in a wider expansion of Region II from the previous embodiment, directly beneath gat 940, resulting in a further reduction in donor impurities underneath the transfer gate 940.

[0031] FIG. 6 illustrates a doping profile in accordance with a third exemplary embodiment of the invention, where a transfer gate 940 is surrounded by a insulating layer 102, formed over a substrate 915, which also having an implanted floating diffusion region 702. Region 930C in FIG. 6 represents the diode region formed subsequent to the three-implant process described above, wherein the implant angles of PD1-PD3 are set at θ_1=5° for PD1(see FIG. 3A), θ_2=30° for PD2 (see FIG. 3B), and θ_3=5° for PD1 (see FIG. 3C). FIG. 6 also shows four concentration regions (I-IV) that are formed in the substrate as a result of the diode region 930C formed by the three implants at the specified implant angles (θ_1=5°, θ_2=30°, and θ_3=5°).

[0032] Region I, generally defined by the region above 132 and below regions 104 and floating diffusion 702, has the largest donor concentration between the range of just over 5E16 /cm^3 to 5E17/cm^3. Region II, generally defined by the region between 127 and 132, has a lesser donor concentration between the ranges of just over 5E15/cm^3 to 5E16/cm^3. Region III, generally defined by the region between 122 and 127, has yet a smaller donor concentration between the ranges of just over 1E14/cm^3 to 5E15/cm^3. Region IV, generally defined by the region below 122, contains the lowest donor concentration at or below 1E14/cm^3. As can be seen in the electrostatic potential contour, the reduction of the implant angles θ_3 from 15° to 5°, and the increase of implant angle θ_2 from 5° to 30° from the previous embodiment has resulted in even a wider expansion of Region II from the previous embodiment, directly beneath gat 940, resulting in a further reduction in donor impurities underneath the transfer gate 940.

[0033] FIG. 7 illustrates a doping profile in accordance with a fourth exemplary embodiment of the invention. Region 930D in FIG. 7 represents the diode formed subsequent to the three-implant process described above, wherein the implant angles of PD1-PD3 are set at θ_1=5° for PD1(see FIG. 3A), θ_2=15° for PD2 (see FIG. 3B), and θ_3=5° for PD1 (see FIG. 3C). FIG. 7 also shows four concentration regions (I-IV) that are formed in the substrate as a result of the diode region 930D formed by the three implants at the specified implant angles (θ_1=5°, θ_2=15°, and θ_3=5°).

[0034] Region I, generally defined by the region above 133 and below regions 104 and floating diffusion 702, has the largest donor concentration between the range of just over 5E16 /cm^3 to 5E17/cm^3. Region II, generally defined by the region between 128 and 133, has a lesser donor concentration between the ranges of just over 5E15/cm^3 to 5E16/cm^3. Region III, generally defined by the region between 123 and 128, has yet a smaller donor concentration between the ranges of just over 1E14/cm^3 to 5E15/cm^3. Region IV, generally defined by the region below 123, contains the lowest donor concentration at or below 1E14/cm^3. The reduction of the implant angles θ_2 from 30° to 15° from the previous embodiment resulted in slightly wider expansion of Region II from the previous embodiment, directly beneath gate 940, resulting in a further reduction in donor impurities underneath the transfer gate 940.

[0035] FIG. 8 illustrates a doping profile concentration in accordance with a fifth exemplary embodiment. Region 930E in FIG. 8 represents the diode region formed subsequent to the three-implant process described above, wherein the implant angles of PD1-PD3 are set at θ_1=5° for PD1(see FIG. 3A), θ_2=5° for PD2 (see FIG. 3B), and θ_3=5° for PD1(see FIG. 3C). FIG. 8 also shows four concentration regions (I-IV) that are formed in the substrate as a result of the diode region 930E formed by the three implants at the specified implant angles (θ_1=5°, θ_2=5°, and θ_3=5°).

[0036] Region I, generally defined by the region above 134 and below regions 104 and floating diffusion 702, has the largest donor concentration between the range of just

over 5E16 /cm^3 to 5E17/cm^3. Region II, generally defined by the region between 129 and 134, has a lesser donor concentration between the range of just over 5E15/cm^3 to 5E16/cm^3. Region III, generally defined by the region between 124 and 129, has yet a smaller donor concentration between the range of just over 1E14/cm^3 to 5E15/cm^3. Region IV, generally defined by the region below 124, contains the lowest donor concentration at or below 1E14/cm^3. As can be seen in the electrostatic potential contour illustration, the reduction of the implant angles θ_2 from 15° to 5° from the previous embodiment has further expanded Region II from the previous embodiment, resulting in an even greater reduction in donor impurities underneath the transfer gate 940.

[0037] A typical processor system which includes a CMOS imager device having pixels constructed according to the present invention is illustrated generally in FIG. 9. A pixel imager array having pixels constructed as described above may be used in an imager device having associated circuits for reading images captured by the pixel array. The imager device may, in turn, be coupled to a processor system for further image processing.

[0038] As can be seen from the process depicted in FIGs. 3A-3C and 3A-3D and in the specific examples, a portion of the implanted photo-diode region 930 which is deeper into substrate 915 extends as much or less towards the transfer gate 940, than a portion of the implanted photodiode region which does not extend as deep into the substrate. This reduces any short channel effect, as well as any associated transfer gate leakage, as compared to the photodiode implant depicted in FIG. 2.

[0039] A processor system which uses a CMOS imager having pixels fabricated in accordance with the invention, for example, generally comprises a central processing unit (CPU) 1544 that communicates with an input/output (I/O) device 1546 over a bus 1552. The CMOS imager 1510 also communicates with the system over bus 1552. The computer system 1500 also includes random access memory (RAM) 1548, and, in the case of a computer system may include peripheral devices such as a floppy disk drive 1554 and a compact disk (CD) ROM drive 1556 which also communicate with CPU 1544 over the bus 1552. As described above, CMOS imager 1510 is combined with a pipelined JPEG compression module in a single integrated circuit.

[0040] It should again be noted that although the invention has been described with specific reference to CMOS imaging circuits having a photodiode and a floating diffusion, the invention has broader applicability and may be used in forming a photodiode structure adjacent a transfer gate in any CMOS imaging apparatus. For example, the CMOS imager array can be formed on a single chip together with the logic or the logic and array may be formed on separate IC chips. In addition to transfer gates, the configuration is equally applicable to other gates, such as reset gates, global shutter, storage gate, high dynamic range gate, etc. Moreover, the implantation process described above is but one method of many that could be used. The implantation process can further be implemented on a variety of image pixel circuits, including three transistor (3T), four transistor (4T) five transistor (5T), six transistor (6T) or seven transistor (7T) structures. Accordingly, the above description and accompanying drawings are only illustrative of preferred embodiments which can achieve the features and advantages of the present invention. It is

not intended that the invention be limited to the embodiments shown and described in detail herein. The invention is only limited by the scope of the following claims.